Realization of Basic Logic Gates using Quantum Dot Cellular Automata Based Reversible Universal Gate

Saroj Kumar Chandra and Prince Kumar Sahu

Abstract--- *Quantum-dot Cellular Automata (QCA) is a new technology for development of logic circuits based on nanotechnology, and it is a one of the alternative for designing high performance computing over existing CMOS technology. The basic logic in QCA does not use voltage level for logic representation rather it represent binary state by polarization of electrons on the Quantum Cell which is basic building block of QCA. Extensive work is going on QCA for circuit design due to low power consumption and regularity in the circuit. Reversible logic design is a well-known paradigm in digital computation, and in this paper we are presenting realization of basic logic gates using the Reversible Universal Gate (RUG).*

Keywords--- *Reversible Universal Gate, Quantum Cell, Quantum Dot Cellular Automata*

I. Introduction

DUE to the miniaturization of transistors, the basic building unit of digital circuits in VLSI technology such as CMOS, the performance of computer chips has shown outstanding development in the last decades. CMOS technology represents binary information by switching the electric current [1] [2] [3] [4]. However, this paradigm has serious drawbacks as device sizes are reduced. The interconnection of devices and signals is one of these problems. Another problem is with regard to the quantization of charge, which becomes significant as transistors become smaller. Finally, current switching results in huge energy dissipation. Recent studies show that the spatial limits of conventional electronics will be reached in the next few years and, as a consequence, this continuing development of VLSI technology is threatened, new approach is required in the circuit design. Quantum-Dot Cellular Automata (QCA) is one of the most promising alternatives nanotechnologies to the CMOS-VLSI technologies [3].

One of the most pressing hurdles in the development of innovative computation paradigms and systems is energy dissipation [5] [6]. A possible solution is reversible computing. QCA is a promising emerging Nanotechnology that relies on novel design concepts. The basic logic devices for QCA are the majority voter (MV) and inverter (INV) [1]. QCA cells and some simple devices have already been successfully developed [7], [8], [9]. A four-phase clocking scheme for QCA also known as Landauer clocking has been proposed in [10]. Based on this clocking scheme, combinational as well as sequential logic design in QCA has been proposed in [1]. QCA has very low power consumption. So, QCA has been deemed as a promising technology for building reversible systems. Many reversible circuits has been proposed using QCA in which Reversible Universal Gate (RUG) [11] is one using which any combinational and sequential circuits can be designed so in this paper we are realizing all basic logic gates using reversible universal gate (RUG).

II. Reversible Gate

A logic gate L is reversible if, for any output Y, there is a unique input X such that

$$L(X) = Y$$

If a gate L is reversible, there is an inverse gate L′ which maps Y to X for which

$$L'(Y) = X.$$

From common logic gates, NOT gate is reversible, as can be seen from its truth table below.

Table 1: Truth Table for Not Gate

INPUT	OUTPUT
0	1
1	0

The original motivation was that reversible gates dissipate less heat (or, in principle, no heat). In a normal gate, input states are lost, since less information is present in the output than was present at the input. This loss of information loses energy to the surrounding area as heat, because of thermodynamic entropy. Another way to understand this is that charges on a circuit are grounded and thus flow away, taking a small charge of energy with them when they change state. A reversible gate only moves the states around, and since no information is lost, so energy is conserved. Any reversible gate must have the same number of input and output bits, by the pigeonhole principle - For one input bit there are two possible reversible gates. One of them is NOT and the other is the identity gate which maps its input to the output unchanged. Many reversible gate exists namely Fredkin, Toffoli,

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QCA1,QCA2 RUG, in which RUG is Universal Gate and use's much less number of QCA cells.

III. Reversible Universal Gate (RUG)

Reversible Universal Gate has a 3-bit input and 3-bit output. First output is majority function, second output is Universal function and its third output is XOR function. The output of RUG gate can be described as mapping bits A,B and C to AB+BC+CA, AB+A'C' and B'C+BC' respectively as shown in figure 1.

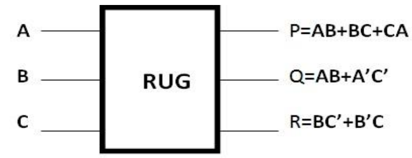

Figure 1: Block Diagram of RUG Gate

QCA cell layout of the RUG is shown in figure 2 using four-phase clocking scheme

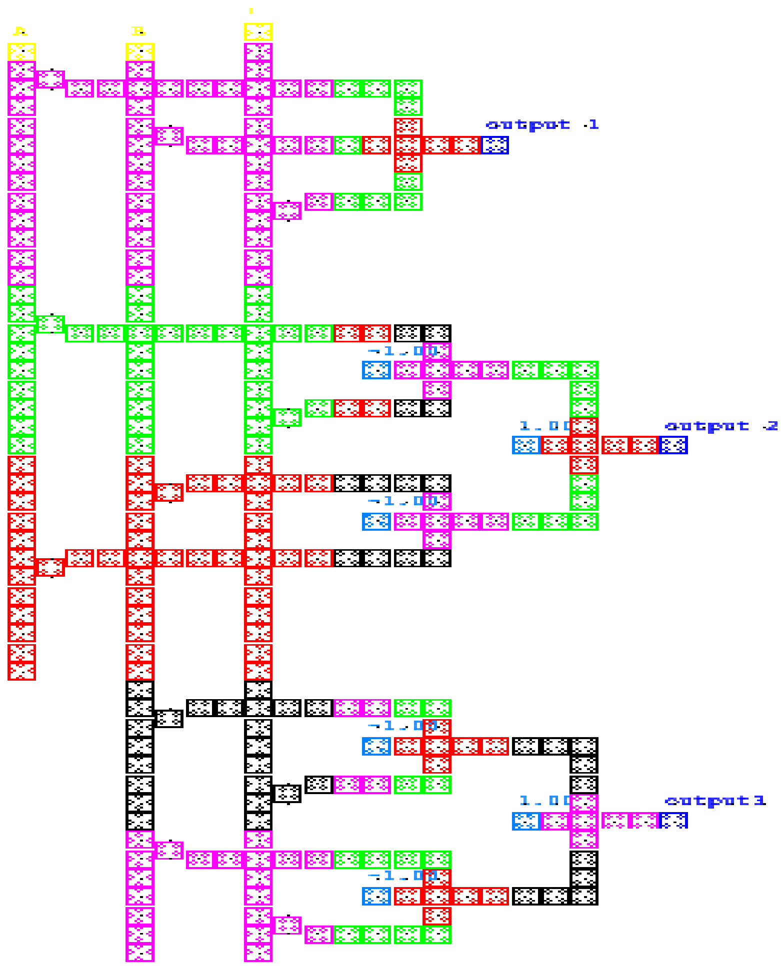

Figure 2: QCA Layout of RUG Gate Using QCA Designer

RUG logic design is consist of seven majority gates (MV) and four inverter, as shown in figure 2 retains in the simple clocking scheme. For the wire A, B, C it is in different clock zone because to main signal strength. Similarly all MV's also kept in corresponding clock zones.

Output OF RUG Gate using QCADesigner of is shown in figure 3 using four-phase clocking.

The RUG gate is universal; this means that for any Boolean function f($x_1, x_2, x_3, \ldots x_m$), there is a circuit consisting of RUG gates which takes $x_1, x_2, x_3, \ldots x_m$ and some extra bits set to 0 or 1 and outputs $x_1, x_2, x_3, \ldots x_m$, f($x_1, x_2, x_3, \ldots x_m$), and some extra bits.

Essentially, this means that one can use RUG gates to build systems that will perform any desired Boolean function computation in a reversible manner. So in this paper we are showing how to realize basic logic gates using RUG.

A Universal Function is a function which can achieve any logic with a given number of variables with minimum number of wire crossings [12]. So from [12], presence of universal function RUG based QCA circuits are very much cost-effective in terms of number of logic gate, wire crossing, cells count as compared to the designs based on existing reversible gate. This is the concept of a special form of reversible logic with universal functionality.

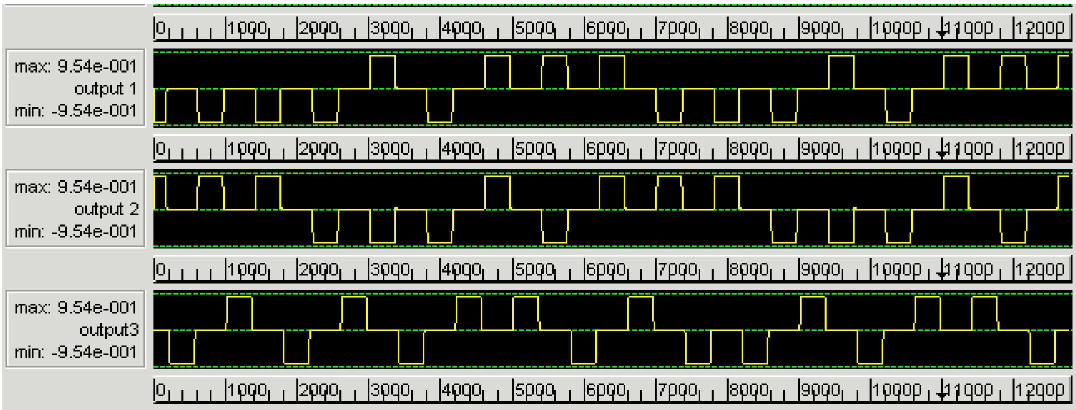

Figure 3: Output of RUG Gate using QCA Designer

IV. REALIZING BASIC LOGIC GATES USING RUG

The RUG gate takes three input bit A, B, C and produces three bit P, Q, R as output as shown in figure:1; using various input combination we can form basic logic gates as output. We are showing how to realize basic logic gates using RUG

A. AND, NOT, XOR Gate Realization

The logic AND,NOT and XOR gate can be realized by giving 0 B and A as input in respective position in RUG gate as shown in figure 4.

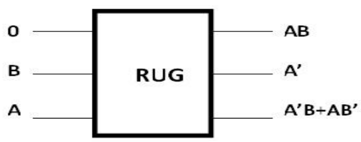

Figure 4: Logic AND Gate

B. OR Gate Realization

The logic OR gate can be realized by giving 1 A and B as input in respective position in RUG gate as shown in figure 5.

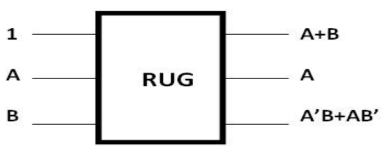

Figure 5: Logic OR Gate

As shown in the above figure that Logic OR can be implemented using RUG gate in single stage and also it implements another gates namely XOR and buffer to pass the input to output.

C. NAND, NOR Gate Realization

The logic NOR and NAND gate can be realized by giving A' B, and 1 as input in respective position in RUG gate as shown in figure 6.

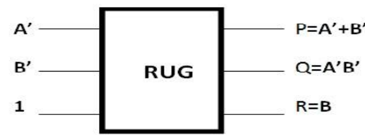

Figure 6: Logic NAND and NOR Gate

Table 2: Summary Table for Input and Output Combination Using Rug

A B C	P=AB+BC+CA	Q=AB+A'C'	R=BC'+B'C	LOGIC GATES
0 A B	AB	B'	AB'+A'B	HALF ADDER/AND,NOT,XOR
1 A B	A+B	A	AB'+A'B	OR,PASS,XOR
A 0 B	AB	A'B'	B	AND,NOR,PASS
A' B' 1	A'+B'	A'B'	B	NAND,NOR,PASS

V. CONCLUSION

RUG is a 3X3 input output reversible logic gate having majority function and universal function and XOR function as outputs; Like any other reversible gates RUG do not erase information and ultimately it leads high performance computing. In this paper we have shown how to realize basic logic gates using RUG. Further this RUG gate can be used to realize all standard functions as well as symmetric function with better cost-effective results in terms of number of logic gate, wire crossings, cells count as compared to the designs based on existing reversible gates..

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