Soft Switching Techniques for High Voltage Gain in Asymmetrical Full Bridge Converter

Nayana G. Nair and T.S. Angel

***Abstract*—*This paper explore the techniques of Asymmetrical full bridge converter with high voltage gain. It achieved zero voltage switching of all power switches, zero current switching of output diodes. Prototype of the converter is developed, experimented and validated using the asymmetrical pulse width modulation techniques. The proposed converter achieved a gain of 12 with zero switching losses, no conduction losses and a fixed switching frequency.*

***Keywords*—*Asymmetrical full bridge converter, soft switching, zero voltage switching (ZVS), zero current switching (ZCS).*

I. INTRODUCTION

THE full bridge asymmetrical zero voltage switching is the popular topology for DC DC converters with a fixed switching frequency, zero switching and high gain. The major field of application of these type converters lies in electric vehicle, UPS, fuel cell, photovoltaic system etc [1]. It is used as an intersize system between the low voltage sources and load which requires high voltage conventional boost converters, which were used in these applications have certain drawback like it requires extreme duty cycle to obtain high voltage gain and its voltage gain is limited due to its parasitic components. Another drawback of the conventional boost converters is the reverse recovery problem of the output diodes which degrades the system performances such as efficiency and electric magnetic noises.

High step up DC DC converters using coupled inductors were introduced to overcome the drawback of conventional boost converters. But due to the leakage inductance of the coupled inductor there were parasitic oscillations across the switches and diodes. Galvanic isolation between the input and output stages of these power converters are a major concern about the safety aspects. These high step up DC DC converters are designed as current fed converters. Due to this the voltage stresses of the switches are severe and hence active snubbers are used to clamp the voltage across the switches and to provide zero voltage switching (ZVS) [2]. But the presence of these active snubbers requires additional switches and hence causes additional conduction losses and thus a decrease in the system frequency.

Voltage-fed converters such as phase-shift full-bridge (PSFB) converters [3], are the solutions to overcome the drawback of current fed converters. The problem of high voltage stress across the switches and diodes are eliminated here and hence zero voltage switching is achieved. But here also exist drawback like large conduction loss due to circulating current, duty cycle loss and voltage spikes across output rectifiers. Even though auxiliary snubber circuits can be used to overcome the problem of large voltage spikes of the output rectifiers, the complexity and the overall cost are increased and system efficiency decreased due to additional circuits.

Overall system efficiency can be increased by using Asymmetrical Pulse Width Modulation (APWM) technique [4]. Here the advantages are zero switching loss, no conduction loss penalty and fixed switching frequency. But again drawback exist like the maximum duty cycle is limited to 0.5 and it require large turns ratio of transformer. Later APWM control scheme for the asymmetrical full-bridge converter was introduced without considering the transformer turns ratio. These were also called buck type converters but they are not suitable for step up applications.

As a solution to the entire problems asymmetrical full bridge converter is proposed. This asymmetrical pulse width modulation technique have advantages like high voltage gain with fixed switching frequency, soft switching operation of all power switches and diodes and clamped voltage power switches and output diodes. There is no reverse recovery problem of the output diodes and limitation of maximum duty cycle disappears.

II. CIRCUT DESCRIPTION

The block diagram representation of the proposed converter is shown in Fig. 1.

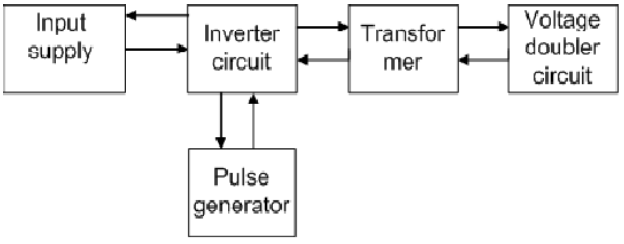

Fig. 1. Block diagram representation of the proposed converter

It consist of 4 blocks namely i) input D.C supply in which a 48 volt supply is given ii) inverter circuit which converts D.C to A.C iii) transformer is used here to step up the voltage along with the voltage doubler circuit iv) voltage doubler circuit and v) pulse generation part.

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ISBN 978-93-82338-65-9

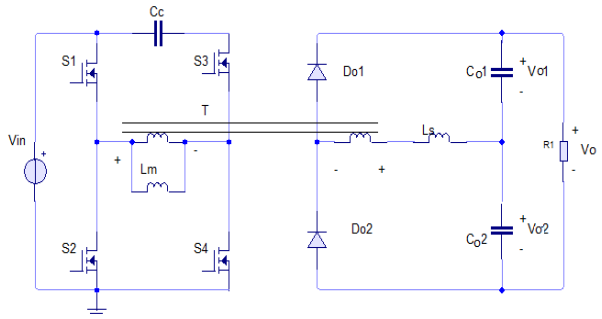

Fig. 2. Circuit diagram

The circuit diagram of the proposed converter with high-voltage gain is shown in Fig. 2. The converter consists of four switches S_1 through S_4. The voltages across the switches S_1 and S_2 in the first bridge are confined to the input voltage V_{in}. The clamping capacitor C_c can clamp the voltages across the switches S_3 and S_4 in the second bridge. The output stage consist of a voltage doubler structure that consists of the secondary winding N_2 of the transformer T, the serial inductor L_s, the output capacitors C_{o1} and C_{o2}, and the output diodes D_{o1} and D_{o2}. According to the voltage doubler structure, the voltage gain increases and the voltage stresses of the output diodes are confined to the output voltage V_o without any auxiliary circuits. The transformer T is modeled as the magnetizing inductance L_m and the ideal transformer that has a turns ratio of 1:n ($n=N_2/N_1$). Its leakage inductance is included in the serial inductor L_s. The voltage across the capacitance C_{o1} in the secondary side is V_{o1} and the voltage across the capacitance C_{o2} is V_{o2}.The output voltage is the sum of V_{o1} and V_{o2}.

The main advantages of the proposed converter include the elimination of switching losses and it maintains low conduction loss and improves the efficiency. It provides high voltage gain at fixed switching frequency. It allows the soft switching operations [5]-[6] of all power switches and diodes thus reverse recovery problem is alleviated due to an additional inductor in the secondary side of the transformer.

III. MODAL ANALYSIS

The operations of the proposed converter during switching period Ts are divided into four modes and that can be explained with the help of Fig. 3.

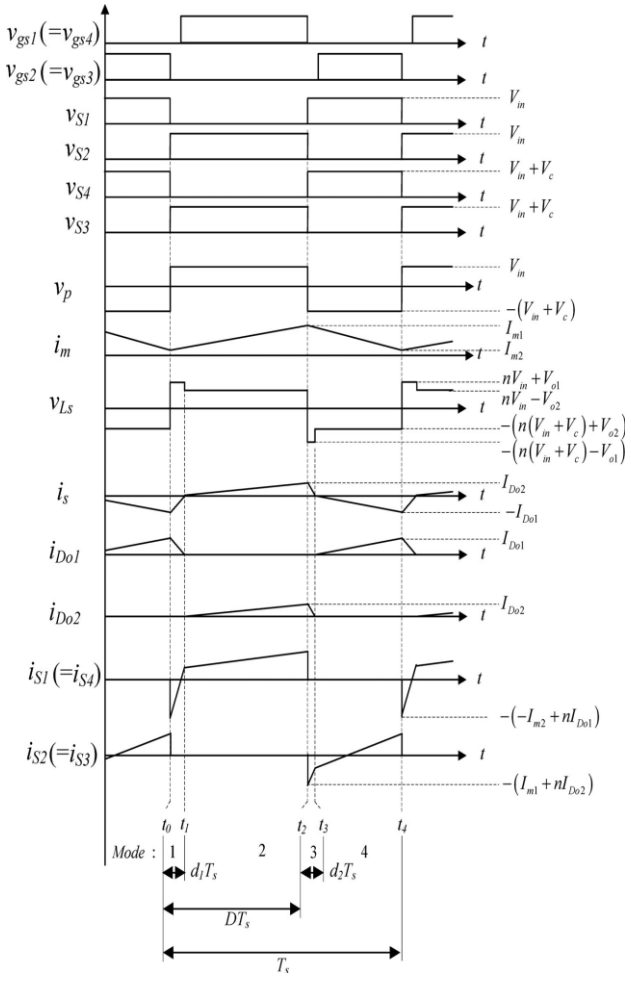

Fig. 3. Theoretical waveforms

Mode 1 [t_0, t_1]:

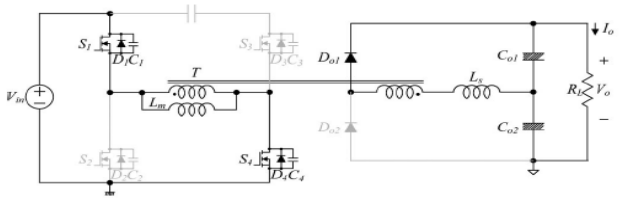

Fig. 4. Mode 1 operation

Mode 1 operation of the proposed converter is shown in Fig. 4. The voltages across the parasitic capacitances C_1 through C_4 are V_{S1}, V_{S2}, V_{S3} and V_{S4}. At t_0, the switches S_2 and S_3 are turned OFF. Then, the energy stored in the magnetic components starts to charge/discharge the parasitic capacitances C_1 through C_4. Therefore, the voltages across C_2 and C_3 start to rise from zero and the voltage V_{S4} starts to fall from ($V_{in}+V_c$) and the voltage v_{S1} starts to fall from V_{in}. When the voltages v_{S1} and v_{S4} arrive at zero, their body diodes D_1 and D_4 are turned ON. Then, the gate signals are applied to the switches S_1 and S_4. Since the currents have already flown through D_1 and D_4 and the voltages V_{S1} and V_{S4} are clamped as zero before the switches S_1 and S_4 are turned ON, zero-

ISBN 978-93-82338-65-9

voltage turn-ON of S_1 and S_4 is achieved. With the turn-ON of S_1 and S_4, the primary voltage v_p across L_m is V_{in}. Then, the magnetizing current I_m increases linearly from its minimum value I_{m2} as follows:

$$I_m(t) = I_{m_2} + \frac{V_{in}}{L_m}(t - t_0) \quad (1)$$

Since the voltage V_{Ls} across Ls is $nV_{in}+V_{o1}$, the secondary current i_s increases from its minimum value $-I_{Do1}$ as follows:

$$i_s(t) = -i_{Do1} + \frac{nV_{in} + V_{o1}}{L}(t - t_0) \quad (2)$$

Mode 2 [t_1, t_2]:

Mode 2 operation is shown in Fig. 5. At t_1, the current i_s and i_{D01} arrive at zero and the diode D_{o1} is turned OFF. Then, the output diode D_{o2} turned ON and its current increases linearly. Since the current changing rate of D_{o1} is controlled by the serial inductor L_s, its reverse-recovery problem is significantly alleviated. Since the voltage V_{Ls} is $(nV_{in}-V_{o2})$ in this mode, the current i_s are given by

$$i_s(t) = \frac{nV_{in} - V_{o2}}{L_s}(t - t_1) \quad (3)$$

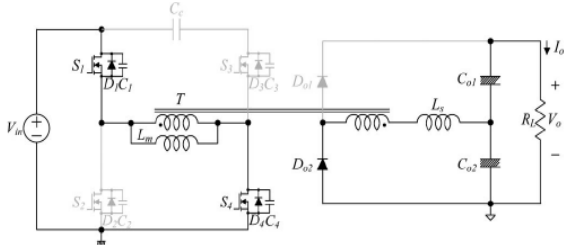

Fig. 5. Mode 2 operation

Mode 3 [t_2, t_3]:

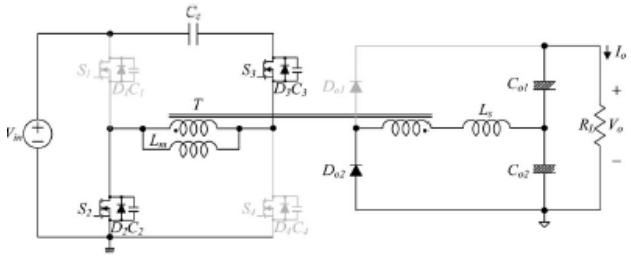

Fig. 6. Mode 3 operation

Mode 3 operation is shown in Fig. 6. Similar to mode 1, the switches S_1 and S_4 are turned OFF at t_2. The parasitic capacitors C_1 and C_4 start to be charged from zero and the capacitors C_2 and C_3 start to be discharged from V_{in} and $(V_{in}+V_c)$ respectively. When C_1 and C_4 are fully charged and discharged, the voltages V_{S2} and V_{S3} become zero and the body diodes D_2 and D_3 are turned ON and the gate signals are applied to the switches S_2 and S_3. Since the currents have already flown through D_2 and D_3 and the voltages v_{S2} and v_{S3} are clamped as zero, zero-voltage turn ON of S_2 and S_3 is achieved. With the turn-ON of S_2 and S_3, the voltage v_p across Lm is $-(V_{in}+V_c)$. Then, the current i_m decreases linearly from its maximum value I_{m1} as follows

$$i_m(t) = I_{m1} - \frac{V_{in} + V_c}{L_m}(t - t_0) \quad (4)$$

Since the voltage v_{Ls} across L_s is $-(n(V_{in} + V_c) + V_{o2})$, the current is decreases from its maximum value I_{Do2} as follows:

$$i_s(t) = -I_{Do2} - \frac{n(V_{in} + V_c) + V_{o2}}{L_s}(t - t_2) \quad (5)$$

Mode 4 [t_3, t_4]:

Mode 4 operation of the proposed converter is shown in Fig. 7.

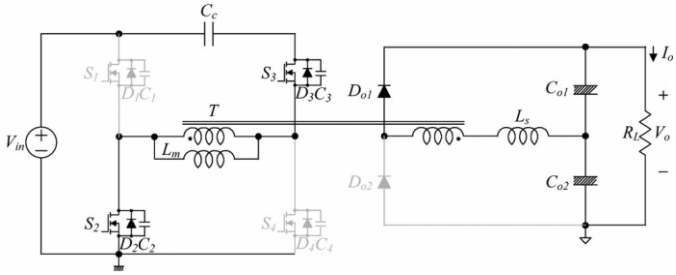

Fig. 7. Mode 4 operation

Similar to mode 2, the currents i_s and i_{Do2} arrive at zero and the diode D_{o2} is turned OFF at t_3. Then, the output diode D_{o1} is turned ON and its current increases linearly. Since the current changing rate of D_{o2} is controlled by L_s, its reverse-recovery problem is significantly alleviated. Since the voltage V_{Ls} is $-(n(V_{in}+V_c)-V_{o1})$, the current is is given by

$$i_s(t) = -\frac{n(V_{in} + V_c) - V_{o1}}{L_s}(t - t_3) \quad (6)$$

At the end of this mode, the currents i_m and i_s arrive at I_{m2} and $-I_{Do1}$, respectively.

IV. DESIGN PARAMETERS

A. *Clamping Capacitor Voltage (V_c)*

Referring to the voltage wave form V_p in Fig. 3, the volt-second balance law gives

$$V_{in}DT_s + (V_{in} + V_c)(1 - D)T_s = 0 \quad (7)$$

B. *Voltage Gain*

The diode currents I_{Do1} can be written as

$$I_{D_{01}} = \frac{nV_{in} + V_{o1}}{L_s} d_1 T_s \quad (8)$$

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The voltage V_{o1} is obtained by

$$V_{o1} = \frac{D - d_1 - (\frac{D}{1-D})d_2}{1 - D + d_1 - d_2} nV_{in} \quad (9)$$

Maximum diode current I_{Do2} can be written as follows:

$$I_{Do2} = \frac{nV_{in} - V_{o2}}{L_s}(D - d_2)T_s \quad (10)$$

Voltage V_{o2} can be obtained by

$$V_{o2} = \frac{D - d_1 - (\frac{D}{1-D})d_2}{D - d_1 + d_2} nV_{in} \quad (11)$$

The average values of the diode currents i_{Do1} and i_{Do2} are equal to the output current I_o and the following relation can be obtained by

$$I_o = \frac{(1 - D - d_1 - d_2)I_{Do1}}{2} \quad (12)$$

From (8) and (12), d_1 and d_2 is obtained by,

$$d_1 = kD \quad (13)$$

$$d_2 = k(1-D) \quad (14)$$

$$k = (1 - \sqrt{1 - \frac{8L_s I_0}{nDV_{in}T_s}}) \quad (15)$$

$$M = \frac{V_0}{V_{in}} \quad (16)$$

C. Maximum and Minimum Values of the Magnetizing Current (im)

In modes 3 and 4, the switch current i_{S3} is flowing through the clamping capacitor C_c. Since the average capacitor current must be zero under a steady-state condition, the average value of i_{S3} is zero. The maximum value I_{m1} and the minimum value I_{m2} are given by

$$I_{m_1} = I_{in} + \frac{V_{in}DT_s}{2L_m} \quad (17)$$

$$I_{m_2} = I_{in} - \frac{V_{in}DT_s}{2L_m} \quad (18)$$

D. ZVS Conditions for the Switches S1 through S4

From Fig. 3, there is no current cancellation between $i_p(=ni_s)$ and i_m at t_2. Therefore, for ZVS of S_2 and S_3, the total energy stored in L_m and L_s should be larger than the energy stored in C_1 through C_4. The following condition should be satisfied:

$$\frac{L_m I^2_{m1}}{2} + \frac{L_s I^2_{Do_2}}{2} > \frac{(C_1 + C_2)V^2_{in}}{2} + \frac{(C_3 + C_4)(V_{in} + V_c)^2}{2} \quad (19)$$

On the other hand, there is current cancellation between $i_p(=ni_s)$ and im at t_0. Therefore, for ZVS of S_1 and S_4, the energy difference between the energies stored in Lm and Ls should be larger than the energy stored in C_1 through C_4 as follows:

$$-\frac{L_{m1}I^2_{m2}}{2} + \frac{L_{s1}D^2_{o1}}{2} > \frac{(C_1 + C_2)V^2_{in}}{2} + \frac{(C_3 + C_4)(V_{in} + V_c)^2}{2} \quad (20)$$

This condition can be used to determine L_m.

E. Voltage Stresses of Power Switches and Output Diodes

The voltage stresses of S_3 and S_4 are the sum of the input voltage V_{in} and the clamping capacitor voltage V_c. Since the clamping capacitor voltage depends on the duty cycle, the voltage stresses of S_3 and S_4 can be changed according to load. Maximum values of V_{S3} and V_{S4} in the second bridge is given by

$$V_{s3,max} = V_{s4,max} = V_{in} + V_c = \frac{DV_{in}}{1 - D} \quad (21)$$

When the duty cycle *D* is below 0.5, the maximum values of V_{S3} and V_{S4} are lower than the input voltage V_{in}. Due to the voltage doubler structure, the maximum values of the voltages across the output diodes are confined to the output voltage V_o.

V. HARDWARE IMPLEMENTATION

In order to verify the validity of the proposed topology, converter prototype is implemented.

TABLE I. PARAMETERS USED

Input Voltage (V_{in})	12 V
Switching Frequency (f_s)	20 kHz
Maximum Duty Cycle (D_{max})	0.7
Serial Inductor (L_s)	570 µH
Maximum output power	150W
Clamping Capacitance (C_c)	22 µF
Values of C_{o1} and C_{o2}	220 µF
MOSFET	IRF830

Hardware part of the proposed converter is shown in Fig. 8 and the parameters used for implementation is given in Table I.

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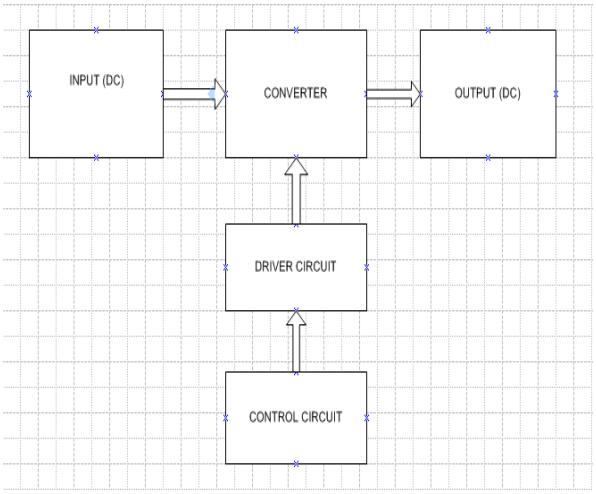

Fig. 8. Hardware part

Here AT89C51 is used and it consists of mainly 4 ports P0, P1, P2 and P3 with 8 pins. Two pins of port 1 are taken for the PWM generation. Controller part is given to the driver circuit and here FAN7392 is used.

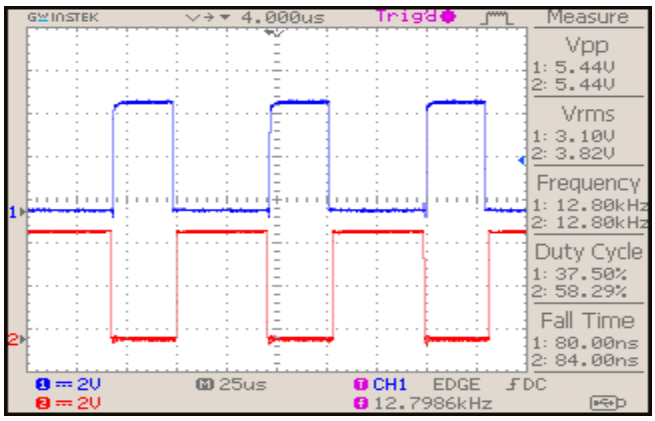

Fig. 9. Pulses during the ON time

Pulses during the ON time are shown in Fig. 9.

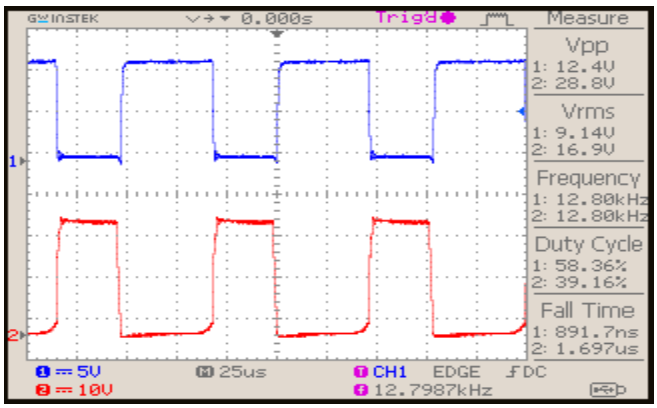

Fig. 10. Voltage across the switches

Voltage across the switches are shown in Fig. 10. Thus the voltage across the first waveform is 12.4 and that of second one is 28.4 with the influence of clamping capacitor.

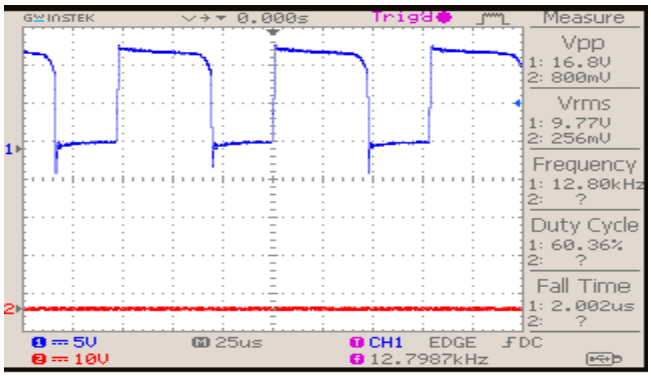

Fig. 12. (a)

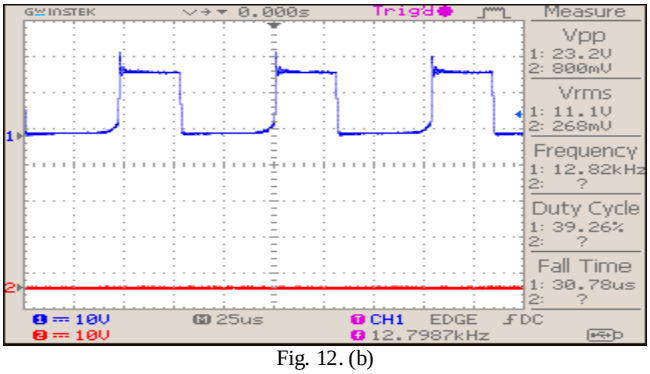

Fig. 12. (b)

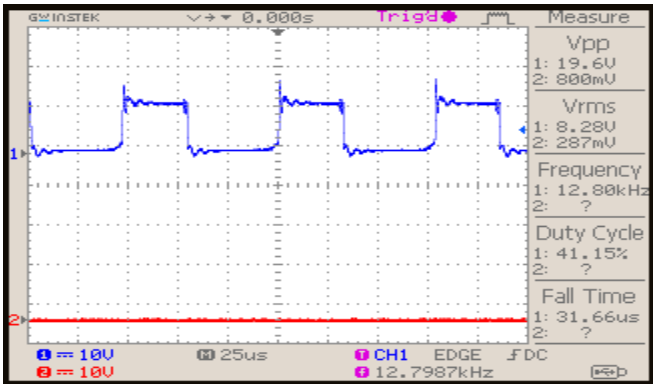

Fig. 12. (c)

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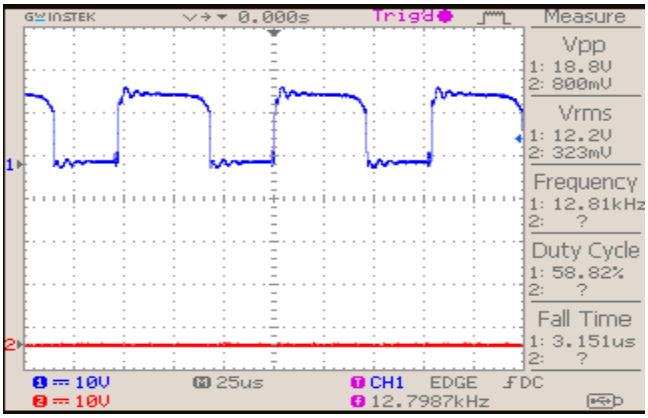

Fig. 12. (d)

Pulses across each switches is shown in the Fig.12. (a), (b), (c) and (d).

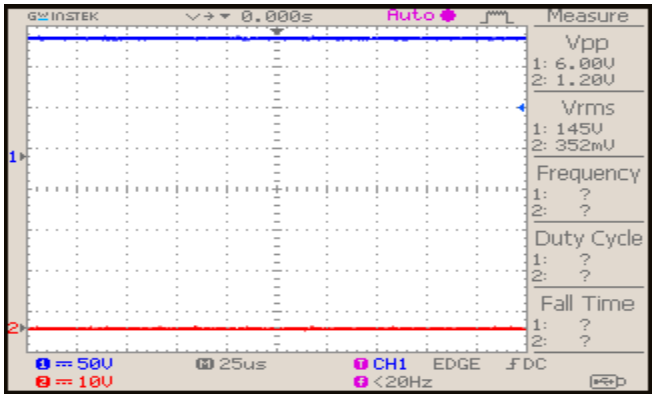

Fig. 13. Output voltage

The output voltage is shown in Fig.13 with 145V as output voltage and input as 12V. Hence the voltage gain of the system is calculated as 12 hence the gain is very high.

VI. CONCLUSION

Asymmetrical full-bridge converter with high voltage gain is proposed in this paper. The ZVS of all power switches and ZCS of the output diodes are achieved. The proposed converter is able to provide high-voltage gain with relatively low transformer turns ratio. Also, without any auxiliary circuits, the voltages across the switches and the output diodes are effectively clamped. Therefore, the proposed converter is suitable for high-voltage applications. The voltage gain is 12 with a transformer turns ratio of 4.5.

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